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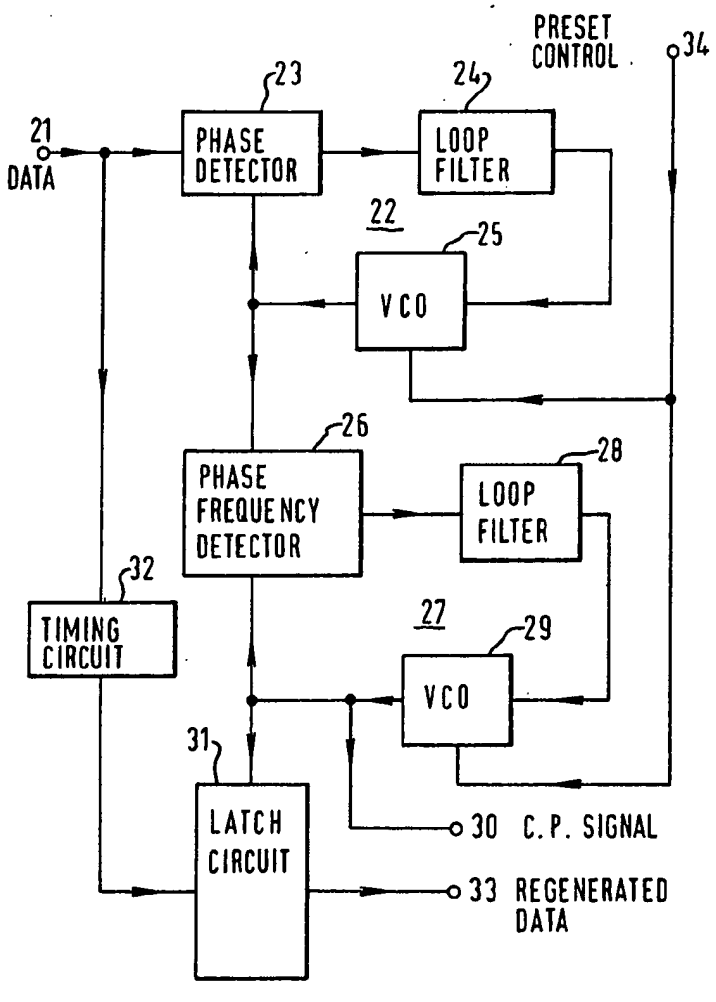
(54) **Apparatus for regenerating a clock pulse signal from a stream of data**

(57) Apparatus for regenerating a clock pulse signal from a stream of data which may be derived from a variable-speed video tape recorder and lacks a strong clock pulse component, comprises a first phase-locked loop circuit 22 to which the incoming data is supplied and which includes a loop filter 24 of relatively wide bandwidth and a voltage controlled oscillator 25. The voltage controlled oscillator 25 supplies a regenerated clock pulse signal to a second phase-locked loop circuit 27 which includes a loop filter 28 of relatively narrow bandwidth and a voltage controlled oscillator 29 which supplies a regenerated output clock pulse signal. The phase-locked loop circuit 22 also includes a phase detector 23, whereas the phase-locked loop circuit 27 also includes a phase frequency detector 26. For a large variation in the data rate, a preset control signal effects coarse control of the VCO frequencies.

FIG. 3.



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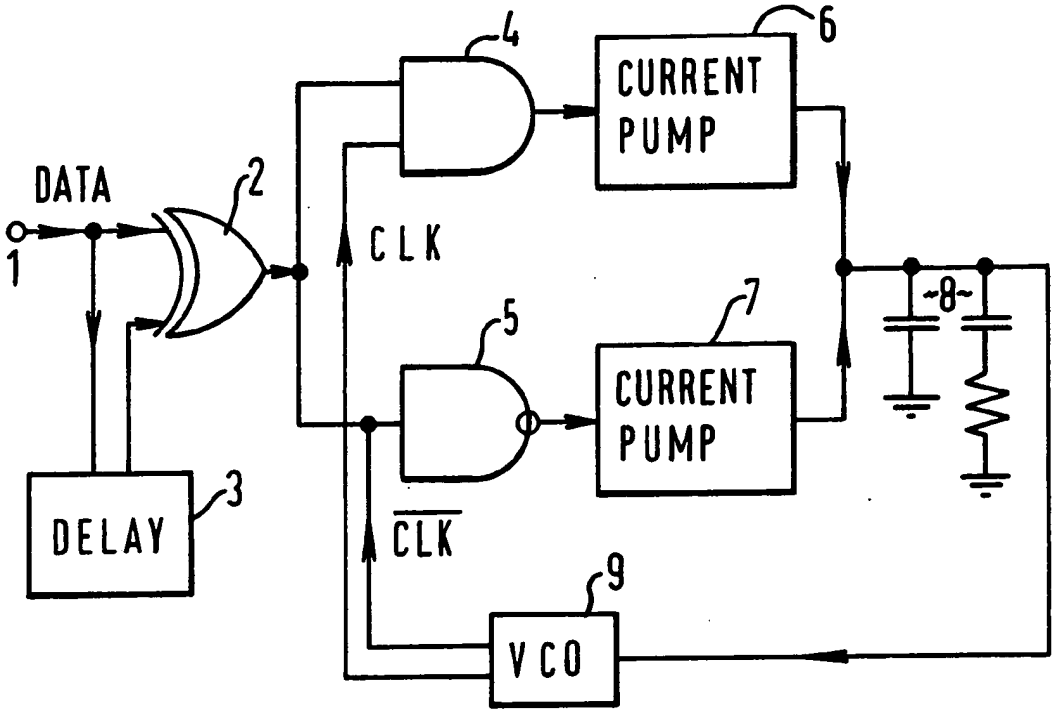
DATA
1
2
CLK
4
CURRENT PUMP
6
5
7
CURRENT PUMP
8
DELAY
3
CLK
9
VCO

FIG. 1.

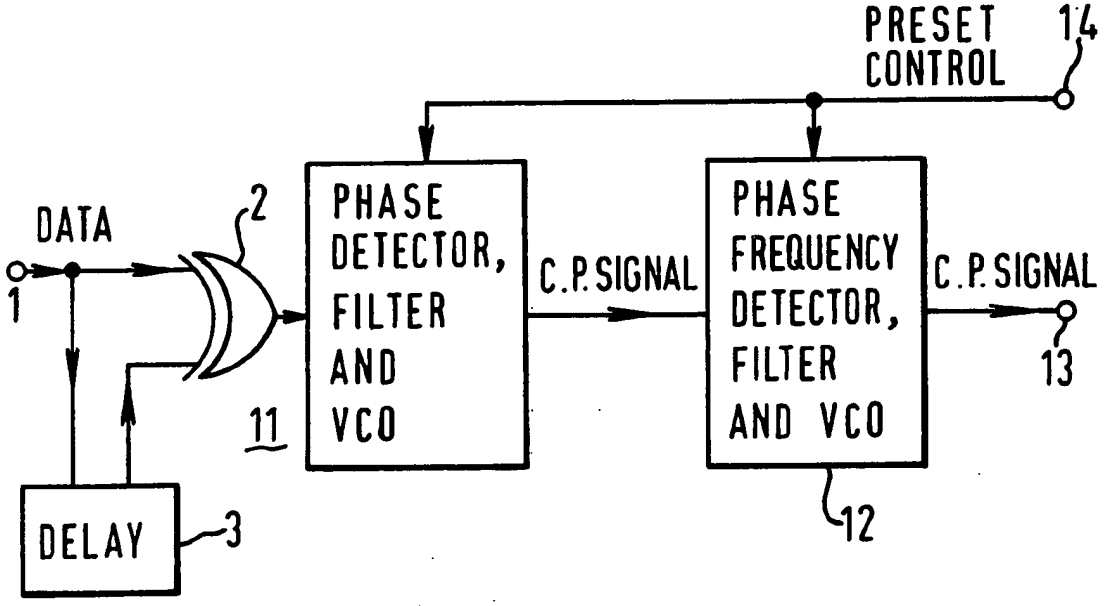
PRESET CONTROL
14
DATA
1
2
PHASE DETECTOR, FILTER AND VCO
11
C.P. SIGNAL
PHASE FREQUENCY DETECTOR, FILTER AND VCO
12
C.P. SIGNAL
13
DELAY
3

FIG. 2.

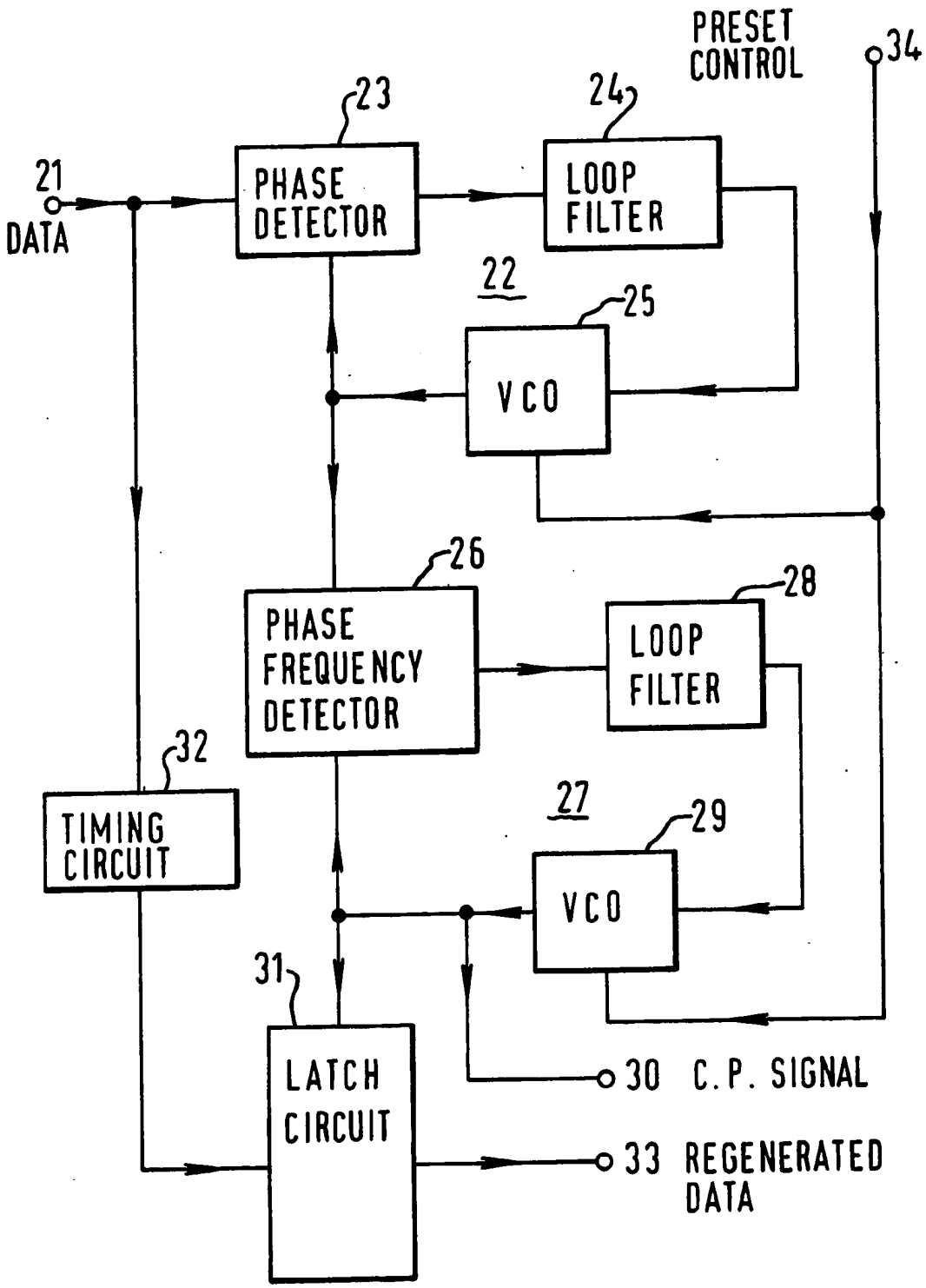
PRESET CONTROL
34
23
24
21
DATA
PHASE DETECTOR
LOOP FILTER
22
25
VCO
26
28
PHASE FREQUENCY DETECTOR
LOOP FILTER
32
TIMING CIRCUIT
27
29
VCO
31
LATCH CIRCUIT
30 C.P. SIGNAL
33 REGENERATED DATA

FIG. 3.

SPECIFICATION

Apparatus for regenerating a clock pulse signal from a stream of data

This invention relates to apparatus for regenerating a clock pulse signal from a stream of data.

Clock recovery is a particular problem where data is being transmitted over a noisy transmission path or is being derived from a noisy source, such as for example off tape from a digital video tape recorder (VTR). Because of the high sampling rate required to digitize a television signal, there is generally no spare capacity available when recording on a digital VTR to record clock information. It is therefore this particular example which will be considered in detail in this specification, although it will be apparent that the application of the invention is not limited to data derived from digital VTRs.

Generally, it has been commonplace to use a tuned circuit for clock regeneration or recovery, the tuned circuit resonating at the clock frequency. However, this technique is only usable in cases where the code used has a strong clock component, that is to say there is a large and reasonably continuous amount of clock information in the incoming data; because if there is a significant gap in the incoming clock information, the tuned circuit will cease to resonate. In the case of digital television signals coming off tape there are substantial gaps in which there is no clock information at all, and a tuned circuit cannot be used. It has therefore been proposed to use a phase-locked loop (PLL) circuit arrangement, but even these have problems as will be discussed in more detail below.

According to the present invention there is provided apparatus for regenerating a clock pulse signal from a stream of data, the apparatus comprising:

a first phase-locked loop circuit to which said stream of data is supplied and including a loop filter of relatively wide bandwidth and a first voltage controlled oscillator for producing a first regenerated clock pulse signal; and a second phase-locked loop circuit to which said first regenerated clock pulse signal is supplied and including a loop filter of relatively narrow bandwidth and a second voltage controlled oscillator for producing an output regenerated clock pulse signal.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows in block form a previously proposed PLL circuit arrangement for clock recovery;

Figure 2 shows in block form an embodiment of the invention;

Figure 3 shows in more detailed block form the embodiment of Figure 2.

Before describing the embodiment, and to assist understanding thereof, further consideration will first be given to previous proposals for clock regeneration. As mentioned above, a tuned circuit is not suitablie for clock regeneration in the case of data derived from a digital VTR. It has therefore been proposed to use a PLL circuit arrangement which can be designed with some of the characteristics of a tuned circuit, in particular a narrow bandwidth and a strong pick-up of the required frequency, but with the additional advantage that in the temporary absence of incoming clock information the PLL circuit can effectively act as a sample-and-hold circuit, with the output continuing at a value determined by the last-received clock information.

In the case of a stream of data derived from the tape of a single-speed digital VTR, each field of the data contains a substantial amount of useful information, but for some 10% of each rotation of the magnetic head assembly of the VTR no useful data is derived because the magnetic head is not engaging the tape. The envelope of the derived data, which envelope has a frequency of 50 Hz, therefore includes some 90% with useful clock information, although even in this part of the envelope there may be significant gaps in the clock information due to drop-out on reproduction or to the characteristics of the actual picture content represented by the data. The PLL circuit has the ability to bridge any such gap and to pick-up and correct quickly to any change in the clock frequency following such a gap.

Referring to Figure 1, this shows a previously-proposed PLL circuit arrangement for clock regeneration. Data derived from the tape of a single-speed digital VTR is supplied by way of an input terminal 1 to one input of an exclusive-OR gate 2, the incoming data from the input terminal 1 also being supplied by way of a delay device 3 which introduces a delay of t, to a second input of the exclusive-OR gate 2. The output of the exclusive-OR gate 2 is connected to respective inputs of AND gates 4 and 5, the outputs of which, inverted in the case of the AND gate 5, are connected to respective current pump circuits 6 and 7, the outputs of which are connected in common to a loop filter 8. The output of the loop filter 8 is a voltage which is supplied to a voltage controlled oscillator (VCO) 9 which produces a clock signal CLK and also an inverted clock signal $\overline{\text{CLK}}$, the clock frequency being controlled in dependence on the voltage supplied by the loop filter 8. The clock signal CLK and the inverted clock signal $\overline{\text{CLK}}$ are respectively supplied to second input terminals of the AND gates 4 and 5.

The operation is as follows. The exclusive-OR gate 2 and the delay device 3 together have the effect of differentiating the incoming data and at the output of the exclusive-OR gate 2 there are produced pulses of duration t, one such pulse being produced for each edge, both positive and negative, of the incoming data. It is necessary that t be less than, or at most equal to, half the clock period of the incoming data.

If the differential pulses supplied by the exclusive-OR gate 2 to the AND gates 4 and 5 move in phase relation to the clock pulse signal

CLK (or $\overline{CLK}$) one of the AND gates 4 or 5 will produce a wider output pulse than the other. The loop will settle, that is to say become correctly locked, when the edges of the lock pulse signal CLK (or $\overline{CLK}$) are centred in the data pulses supplied by the exclusive-OR gate 2. This part of the circuit arrangement therefore forms a phase detector, and this particular form of phase detector is sometimes called a charge pump phase detector.

The loop filter 8 largely determines the characteristics of the phase-locked loop. In a particular example of the PLL circuit arrangement of Figure 1, the operating frequency is 50 MHz, the hold range is ±500 KHz, the capture range is 1 MHz, the loop bandwidth is 200 KHz and the accuracy of data regeneration is within ±1 nanosecond.

There is, however, a problem, and this is that if the loop filter bandwidth is too small, the PLL circuit can lock out. This occurs when the voltage supplied to the VCO 9 is at one end of the range when it should be at the other. In this case the loop filter 8 integrates the frequency difference and no error is apparent. To overcome this problem the bandwidth of the loop filter 8 must be wide, but the wider this bandwidth is made the less effective the arrangement is in reducing the noise modulation. In the case of data off the tape of a digital VTR, therefore, which data is subject to severe noise modulation, it is rather difficult to find a satisfactory compromise design for the loop filter 8 which will sufficiently reduce the noise modulation without, at the same time, causing lock out.

This difficulty is compounded in the case of a digital VTR the speed of which is to be varied in order to achieve special effects such as fast-motion, slow-motion and stop-motion. Where the normal replay speed results in a data rate of 50 Megabits per second, the special effects may cause the data rate to change to somewhere in the range of 35 to 65 Megabits per second. To overcome this problem the present invention provides a dual PLL circuit arrangement which combines the characteristic of having a very wide lock range and a very narrow filter bandwidth.

An embodiment of the invention is shown in Figure 2 and comprises a first PLL circuit arrangement 11 generally as described above with reference to Figure 1 and a second PLL circuit arrangement 12.

As described above, the incoming data is supplied to the input terminal 1 which is connected directly and by way of the delay device 3 to respective inputs of the exclusive-OR gate 2. The output of the exclusive-OR gate 2 is connected to the remainder of the PLL circuit arrangement comprising the charge pump phase detector, the loop filter and the VCO which are generally as shown in Figure 1 but are not shown separately in Figure 2. The first PLL circuit arrangement 11 produces a regenerated clock pulse signal which is supplied to the input of the second PLL circuit arrangement 12. This regenerated clock pulse signal has too much jitter to be used directly for data regeneration.

The second PLL circuit arrangement 12 comprises a phase frequency detector in the form of digital storage phase detector which can operate with a very narrow frequency bandwidth and does not suffer from lock out, that is, the capture range always equals the lock range. It cannot lock out because it is a phase and frequency detector and not merely a phase detector. Thus, if, for example, the frequency is too low, this is positively indicated. However, the PLL circuit arrangement 12 cannot be used alone, because there is insufficient clock information in the incoming data supplied to the input terminal 1.

As compared with Figure 1, in the embodiment of Figure 2 the first PLL circuit arrangement 11 has been modified to increase the capture range, the hold range and the loop bandwidth each by a factor of six. The effect of this is that the regenerated clock pulse signal supplied by the first PLL circuit arrangement 11 to the second PLL circuit arrangement 12 is insufficiently filtered for direct use, but this regenerated clock pulse signal has the noisy component filtered out to the required bandwidth of 100 KHz by the second PLL circuit arrangement 12, which supplies an output filtered clock pulse signal to an output terminal 13.

Although not shown in Figure 2, the second PLL circuit arrangement 12 comprises the phase frequency detector, a loop filter and a VCO, the latter two elements being generally similar to those shown in Figure 1. The phase frequency detector may be generally as described in "Phase Lock Techniques" by F M Gardner, 2nd Edition Wiley, Page 123 or "Motorola MECL Handbook" 1978, Pages 6—72 to 6—76.

Gross variation in the data rate occasioned by a selection of a different special effect mode causes a VCO pre-set control signal to be supplied to an input terminal 14 for supply to the respective VCOs in the first and second PLL circuit arrangements 11 and 12 to effect coarse control of their operating frequencies. Provision of such a VCO preset control signal eases the circuit design, but is not essential.

A further embodiment will now be described with reference to Figure 3. Data derived from the tape of a variable-speed digital VTR is supplied by way of an input terminal 21 to a first PLL circuit 22 comprising a phase detector 23, a loop filter 24 having a relatively wide bandwidth and a VCO 25. The output supplied by the VCO 25 is a first regenerated clock pulse signal which is supplied to the phase detector 23 and also to a phase frequency detector 26 of a second PLL circuit 27. The second PLL circuit 27 also includes a loop filter 28 having a relatively narrow bandwidth and a VCO 29. The output of the VCO 29 is the required output regenerated clock pulse signal and is supplied to the phase frequency detector 26, to an output terminal 30 and also to a latch circuit 31. The stream of data supplied to the input terminal 21 is also supplied to a timing circuit 32

to effect any required delay and is then supplied to the latch circuit 31 which is latched under control of the regenerated clock pulse signal, so as to supply the required regenerated output data of an output terminal 33. An input terminal 34 is connected to the VCOs 25 and 29 for the supply thereto of a preset control signal as in the embodiment of Figure 2.

Briefly, the operation is as follows. The incoming stream of data which is supplied to the input terminal 21 is derived from a variable-speed VTR, so is deficient in clock information, and moreover may vary in data rate over a fairly substantial range, in particular when the mode of the VTR is changed to achieve a special effect. The bandwidth of the loop filter 24 is however such as to ensure that the PLL circuit 22 has a vary wide capture range. Despite any lack of clock information in the incoming data, therefore, the VCO 25 supplies the continuous first regenerated clock pulse signal to the PLL circuit 27. The bandwidth of the loop filter 28 is such that the PLL circuit 27 has a relatively narrow capture range and the VCO 29 supplies the required output regenerated clock pulse signal.

It is easy to add an error indicator to the embodiment of Figure 2 or Figure 3. This requires a further latch circuit to which are supplied the incoming data and a regenerated clock pulse signal derived from the output of the second PLL circuit arrangement 12 (Figure 2) or the second PLL circuit 27 (Figure 3). Normally the regenerated clock pulse signal latches "0"s through the latch circuit, but should the regenerated clock pulse signal become mistimed relative to the data, that is, be clocking the data on an edge, then the latch circuit clocks a "1". This forms an error pulse which is used to drive a buffer circuit which broadens the pulse sufficiently to energise a visual display. If the clock regenerator fails to lock correctly for any reason the error pulses will occur frequently and the visual display will be substantially continuously energised.

The invention is applicable to other circumstances where data is supplied over a noisy transmission path or is derived from a noisy source. This can arise for example in computers or where a signal is supplied over a radio path which is subjected to fading.

CLAIMS

1. Apparatus for regenerating a clock pulse signal from a stream of data, the apparatus comprising:

a first phase-locked loop circuit to which said stream of data is supplied and including a loop filter of relatively wide bandwidth and a first voltage controlled oscillator for producing a first regenerated clock pulse signal; and a second phase-locked loop circuit to which said regenerated clock pulse signal is supplied and including a loop filter of relatively narrow bandwidth and a second voltage controlled oscillator for producing an output regenerated clock pulse signal.

2. Apparatus according to claim 1 wherein said first phase-locked loop circuit includes a phase detector to which said stream of data is supplied.

3. Apparatus according to claim 2 wherein said second phase-locked loop circuit includes a phase frequency detector to which said first regenerated clock pulse signal is supplied.

4. Apparatus according to claim 1, claim 2 or claim 3 wherein said output regenerated clock pulse signal is supplied to a latch circuit to which said stream of data is also supplied, said latch circuit supplying output regenerated data.

5. Apparatus according to any one of the preceding claims wherein said stream of data is derived from a variable-speed video tape recorder.

6. Apparatus for regenerating a clock pulse signal from a stream of data, the apparatus being substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

7. Apparatus for regenerating a clock pulse signal from a stream of data, the apparatus being substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

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